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A = 1 and B = 1, ☐ B=1, \! B = 1, the latch state is Q = 1, Q=1, Q =

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1, (e) Derive a circuit for the A B AB A B latch using four two-input NOR $\square \setminus \text{text \{NOR\}} \setminus !$ NOR gates and two inverters.

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